

# DATA SHEET

## **74F595**

**8-bit shift register with output latches  
(3-State)**

Product specification

1990 Apr 18

IC15 Data Handbook

## 8-bit shift register with output latches (3-State)

74F595

## FEATURES

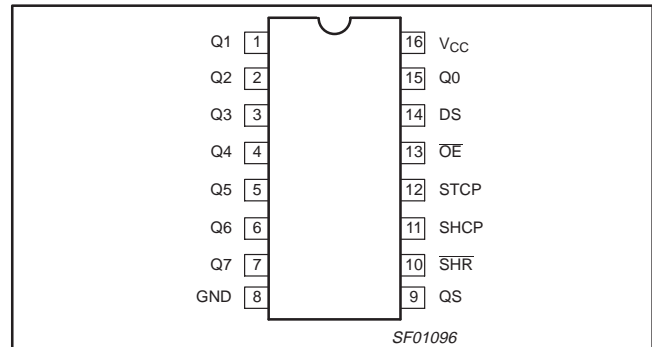
- Low noise, low switching feedthrough current
- Controlled output edge rates
- High impedance PNP base inputs for reduced loading (20 $\mu$ A in High and Low states)
- 8-bit serial-in, parallel-out shift register with storage
- 3-state outputs
- Shift register has direct clear
- Guaranteed shift frequency-DC to 100MHz

## DESCRIPTION

The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-State outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthrough current and controlling both Low-to-High and High-to-Low slew rates.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F595	130MHz	65mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
16-pin plastic DIP	N74F595N	SOT38-4
16-pin plastic SO	N74F595D	SOT109-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS	Serial data input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
Qs	Serial expansion output	50/33	1.0mA/20mA
Q0-Q7	Data outputs	150/40	3.0mA/24mA

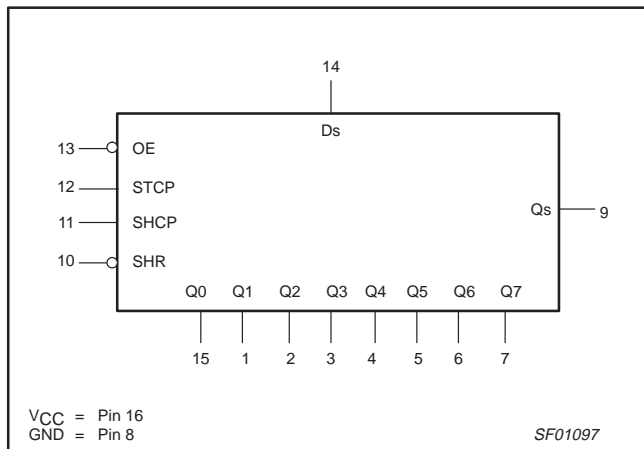
## NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

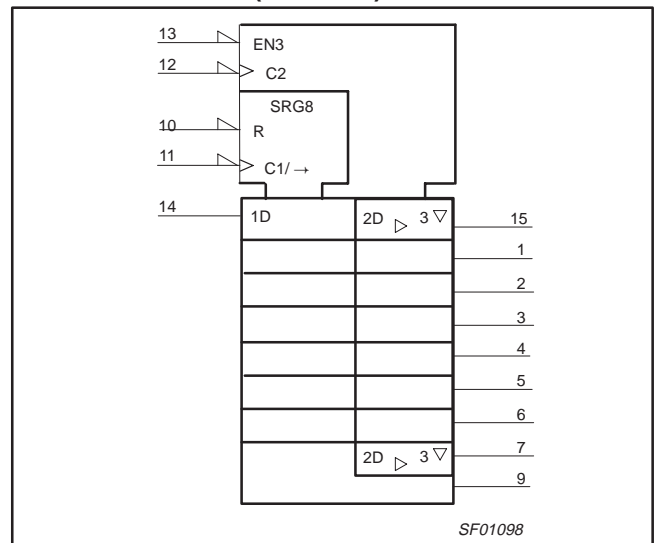
# 8-bit shift register with output latches (3-State)

74F595

## LOGIC SYMBOL



## IEC/IEEE SYMBOL (IEEE/IEC)



## MODE SELECT – FUNCTION TABLE

INPUTS					INTERNAL SHIFT REGISTERS		INTERNAL STORAGE REGISTER	OUTPUTS		OPERATING MODES
OE	SHR	SHCP	STCP	Dn	O0	O1–O7	Q0–Q7	Q0–Q7	QS	
H	H	↑	↑	X	O0	O1–O7	Q0–Q7	Z	Q7	No Change
H	L	X	↑	X	L0	L	Q0–Q7	Z	L	Clear shift register, hold latch
L	L	X	↑	X	L0	L	Q0–Q7	Q0–Q7	L	
H	H	↑	↑	ds	Ds	o0–o6	Q0–Q7	Z	o6	Shift
L	H	↑	↑	ds	Ds	o0–o6	Q0–Q7	Q0–Q7	o6	
H	H	↑	↑	X	O0	O1–O7	o0–o7	Z	Q7	Store
L	H	↑	↑	X	O0	O1–O7	o0–o7	o0–o7	Q7	
H	H	↑	↑	ds	Ds	o0–o6	o0–o7*	Z	o6	Store, then Shift
L	H	↑	↑	ds	Ds	o0–o6	o0–o7*	o0–o*	o6	

H = High voltage level

L = Low voltage level

X = Don't care

Z = High impedance

dn (on)=Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition

↑ = Low-to-High clock transition

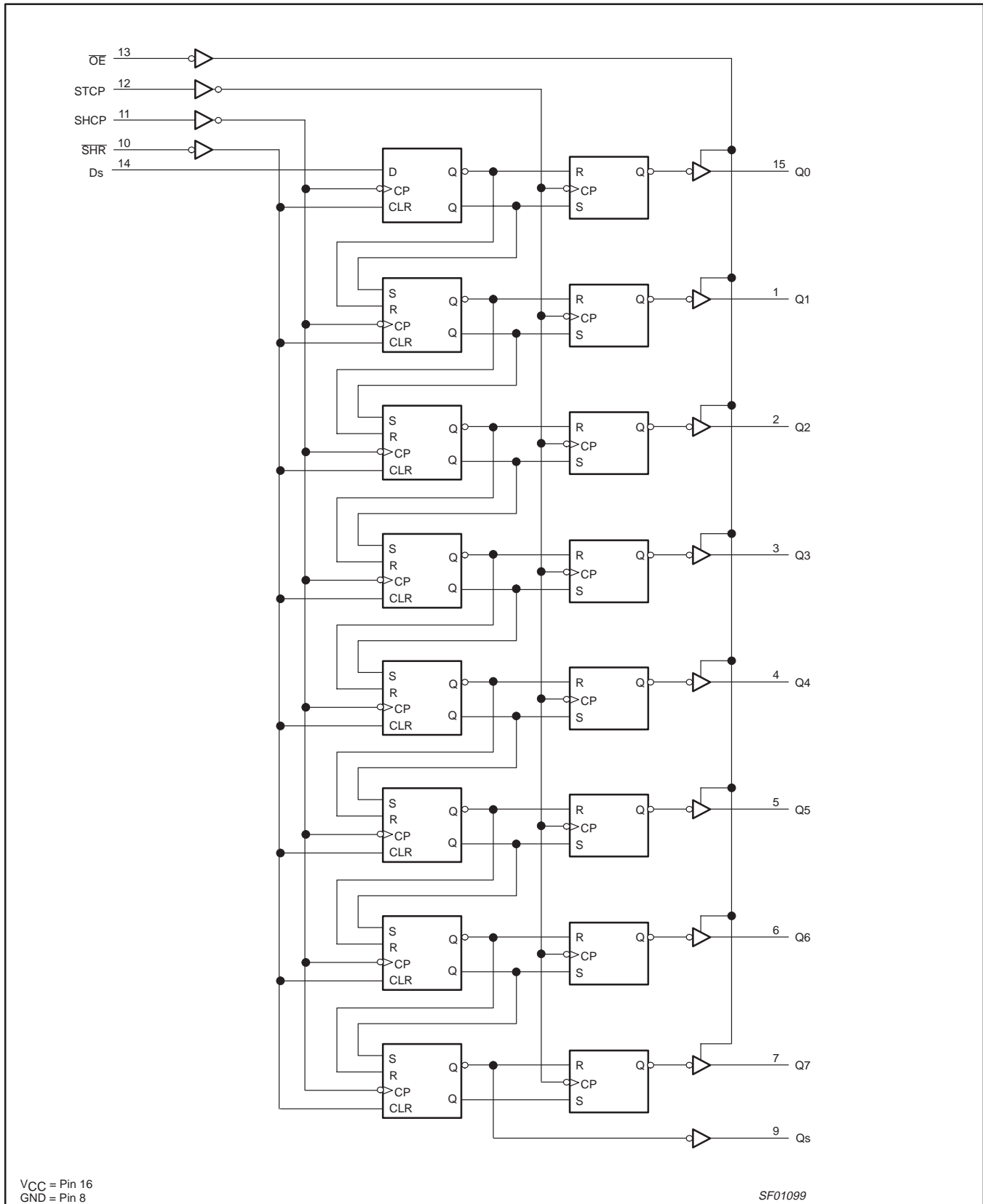
↑̂ = Not a Low-to-High clock transition

\* = When clocking both SHCP and STCP simultaneously the Shift Register state will always be one clock pulse ahead of the Storage Register

# 8-bit shift register with output latches (3-State)

## 74F595

### LOGIC DIAGRAM



## 8-bit shift register with output latches (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage		-0.5 to +7.0	V
I <sub>IN</sub>	Input current		-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state		-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	Qs	40	mA
		Q0-Q7	48	mA
T <sub>amb</sub>	Operating free-air temperature range		0 to +70	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current	Qs		-1	mA
		Q0-Q7		-3	mA
I <sub>OL</sub>	Low-level output current	Qs		20	mA
		Q0-Q7		24	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

## 8-bit shift register with output latches (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>NO TAG</sup>			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V <sub>OH</sub>	High-level output voltage	Qs	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -1mA	±10%V <sub>CC</sub>	2.5			V
					±5%V <sub>CC</sub>	2.7	3.4		V
		Q0-Q7		I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V
					±5%V <sub>CC</sub>	2.7	3.3		V
V <sub>OL</sub>	Low-level output voltage	Qs	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN,	I <sub>OL</sub> = 20mA	±10%V <sub>CC</sub>		0.30	0.50	V
					±5%V <sub>CC</sub>		0.30	0.50	V
		Q0-Q7		I <sub>OL</sub> = 24mA	±10%V <sub>CC</sub>		0.35	0.50	V
					±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA	
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA	
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-20	mA	
I <sub>ozH</sub>	Off-state output current, High level of voltage applied	Q0-Q7 only	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V				50	μA	
I <sub>ozL</sub>	Off-state output current, Low level of voltage applied	Q0-Q7 only	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V				-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>		V <sub>CC</sub> = MAX			-60		-150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				55	80	mA
		I <sub>CCL</sub>					70	100	mA
		I <sub>CCZ</sub>					65	95	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 8-bit shift register with output latches (3-State)

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$f_{MAX}$	Maximum clock frequency—SHCP to Qs	Waveform NO TAG	115	135		90		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay SHCP to Qs	Waveform NO TAG	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.5 7.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay STCP to Q0–Q7	Waveform NO TAG	5.5 3.0	8.0 5.0	10.0 8.0	4.5 3.0	13.0 8.5	ns
$t_{PHL}$	Propagation delay SHR to Qs	Waveform NO TAG	3.5	5.5	8.0	3.0	8.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable time OE to Q0–Q7	Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 10.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable time OE to Q0–Q7	Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.5	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Ds to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Ds to SHCP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Setup time, Low SHR to STCP	Waveform 3	4.5			5.0		ns
$t_s(H)$	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
$t_W(H)$ $t_W(L)$	SHCP Pulse width, High or Low	Waveform NO TAG	3.5 4.0			4.0 4.0		ns
$t_W(H)$ $t_W(L)$	STCP Pulse width, High or Low	Waveform NO TAG	4.0 3.0			4.0 3.5		ns
$t_W(L)$	$\overline{SHR}$ Pulse width, Low	Waveform NO TAG	3.0			3.0		ns
$t_{REC}$	Recovery time, SHR to SHCP	Waveform NO TAG	3.0			3.0		ns

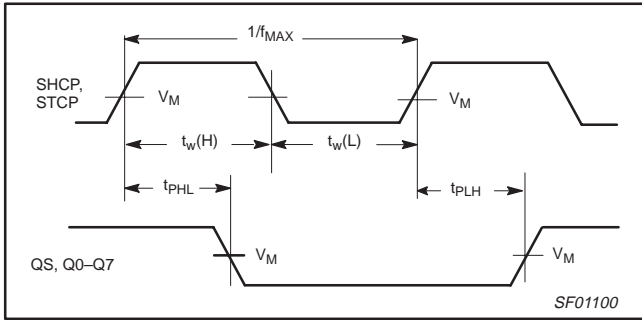
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

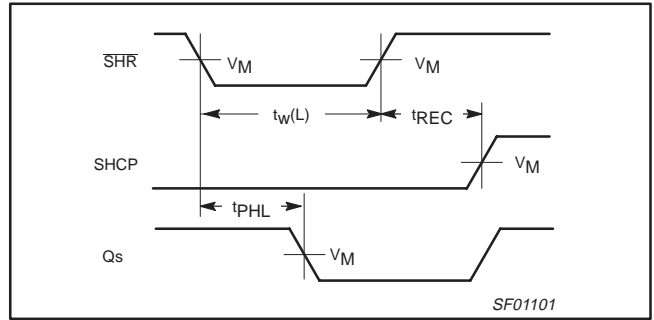
The shaded areas indicate when the input is permitted to change for predictable output performance.

# 8-bit shift register with output latches (3-State)

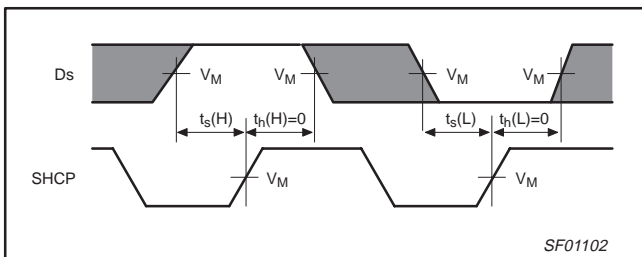
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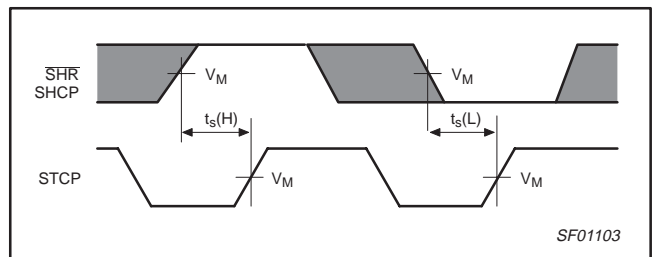
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency**



**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time**



**Waveform 3. Data Setup and Hold Times**



**Waveform 4. Setup and Hold Times**



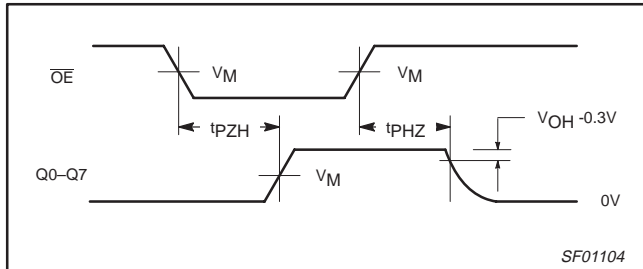
# 8-bit shift register with output latches (3-State)

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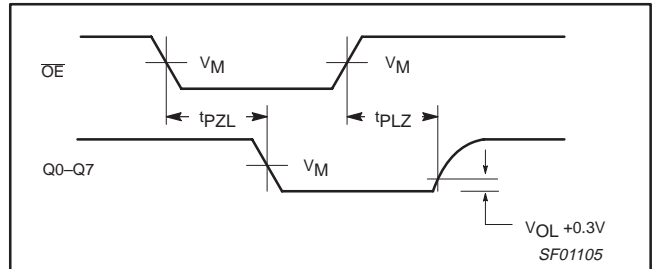
## AC WAVEFORMS (Continued)

For all waveforms,  $V_M = 1.5V$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

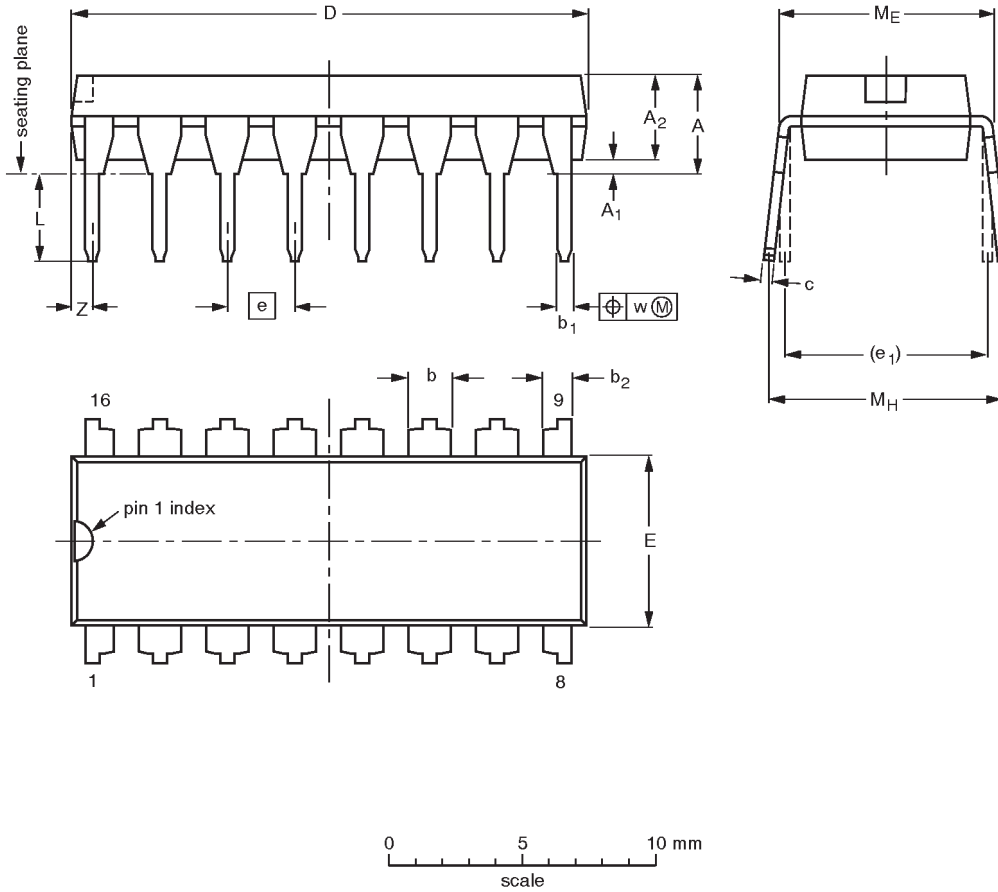
SF00777

8-bit shift register with output latches (3-State)

74F595

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

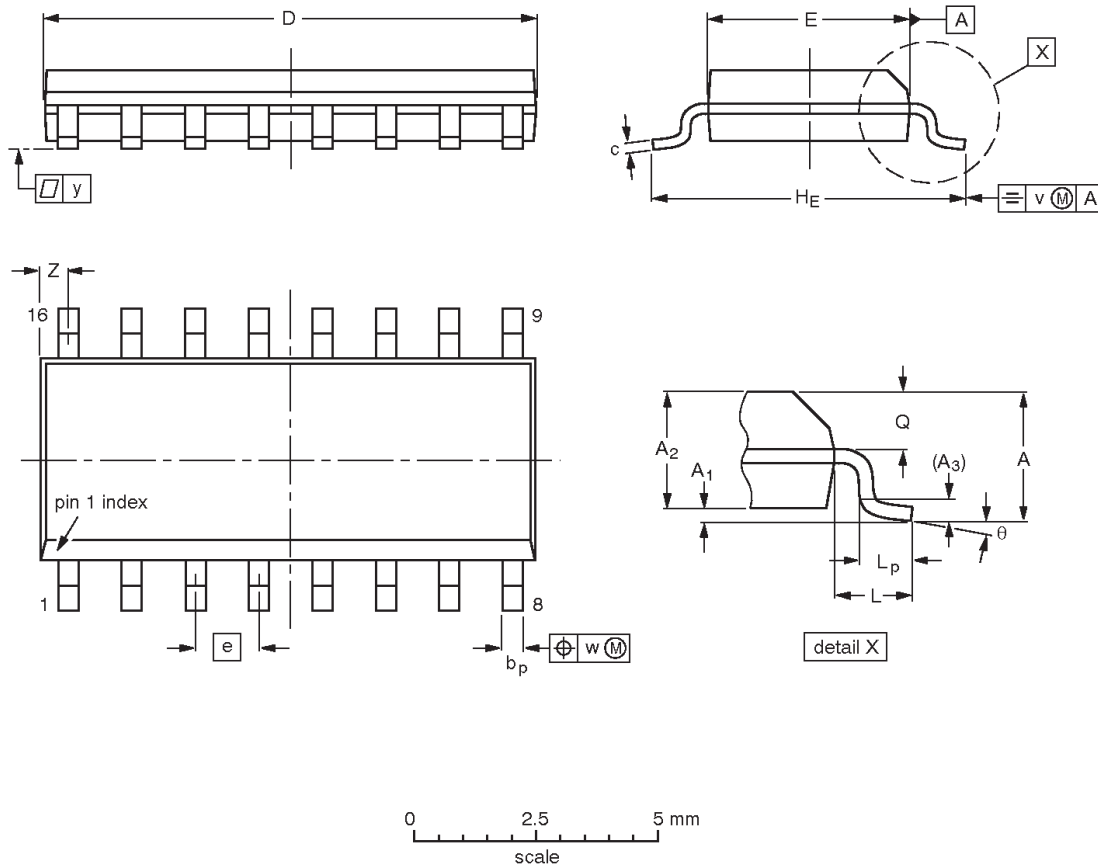
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

# 8-bit shift register with output latches (3-State)

74F595

**SO16:** plastic small outline package; 16 leads; body width 3.9 mm

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 0.049	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.014	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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8-bit shift register with output latches (3-State)

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**NOTES**

## 8-bit shift register with output latches (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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